MEDEA+

Process innovation key to reducing device size and cost

EUREKA

Continuous investment and collaboration

Continuous investment by the semiconductor industry and pre-competitive collaboration between companies in the necessary R&D with the support of European public authorities through EUREKA and national funding programmes have helped in building a strong European supply chain, from material suppliers to equipment manufacturers.

The important role of MEDEA+ and its EUREKA predecessor programmes is well illustrated by the success of the Netherlands-based company ASML. In the last decade, this manufacturer has become the world leader for the photolithography equipment that is essential for modern chip fabrication with net sales of €3.8 billion in 2007 – a 60% global market share. The company spends more than €500 million a year on R&D, mostly in Europe. And not only is it a major employer in the Netherlands, with 75% of its employees involved in R&D, but it also subcontracts 90% of production, again much in Europe

On the materials side, SOITEC – a spin-off from the LETI research centre in France in 1993 – has established itself as the sole supplier of silicon on insulator (SOI), a value-added wafer substrate material now entering the production cycle for state-of-the-art chips. Total revenues in 2007 were €372 million.

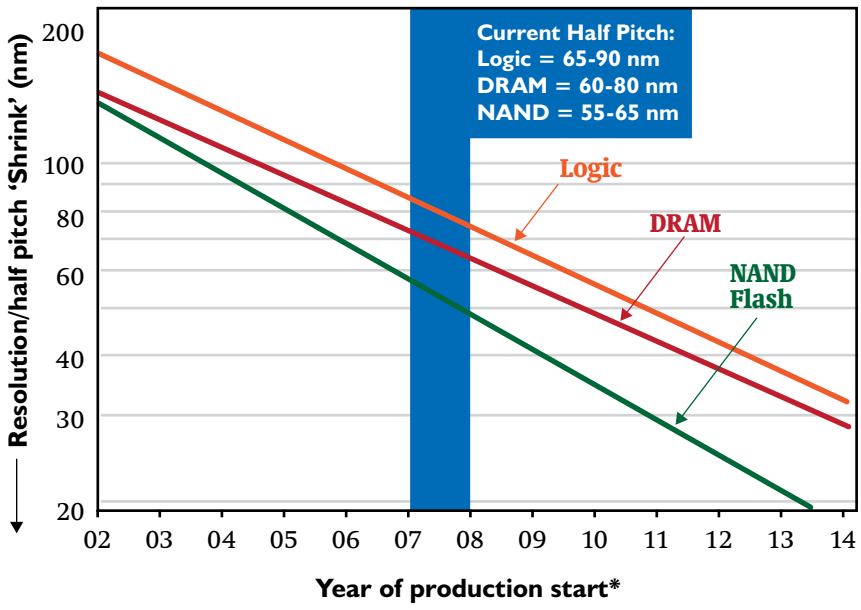
And silicon manufacturer Siltronic had sales of €1.45 billion in 2007 and has 5,600 employees; it is ranked third in the global silicon wafer market, with a 15% market share.

Process innovation key to reducing device size and cost

Success in MEDEA+ projects on developing innovative processing technologies, materials and substrates for 90 and 65 nm nodes has ensured Europe remains in the global vanguard for semiconductor fabrication and is encouraging industry to collaborate in the next steps to the 45 nm and 32 nm nodes. Extensive developments also in process materials and modules from gases to supply-chain optimisation ensure that Europe will continue to be global leader in the technologies essential for the future of the micro- and nanoelectronics industry as well as the wide range of industries – from aerospace and automotive, through wired and wireless communications, to broadcast and multimedia – that depend on these advances.

Innovation is the key driver in the microelectronics industry. One result is that the semiconductor content of the global electronic equipment industry has grown from a mere 2% in the 1960s to 20% today. In the past 30 years, the cost of producing 1 Mbyte of memory has dropped from around €75,000 to just 10 eurocents now. This has come about through innovation and development not only in the chip designs themselves but also in materials, process and manufacturing technologies.

Complete understanding and control of process technology is essential to ensure chips are fabricated on time and right first time. Not only is it necessary to invest in the most cost-effective equipment but also to have the right materials. Moreover, reducing feature sizes in ever smaller chips puts tremendous demands on process cleanliness. All this requires close collaboration between designers, chipmakers, system builders and both equipment and materials suppliers.



Increasing miniaturisation

* *Note: Process development 1.5 - 2 years in advance*

Source ASML

Cleaner production

Significant progress was made in preparing the production infrastructure necessary for the fabrication of integrated circuits with circuit features down to 65 nm in the MEDEA+ T301 0.1 μm Fab project. Key developments included new processing chemicals and gases to meet ever more demanding purity levels as well as improved cleaning processes for wafer and production tools.

Attention was also paid to the change from aluminium to copper interconnects in new chip generations. Copper offers several advantages over aluminium: its higher conductivity simplifies routing, as the number of interconnect levels can be reduced. Interconnect delays are shorter, therefore power demands are lower, allowing for better chip performance – particularly higher speeds – at equal power. Use of the damascene process for metal layer deposition reduces overall chip manufacturing costs by some 30% per interconnect level. However, it was essential to adapt copper technology to large scale manufacture.

Several areas critical to 90 and/or 65 nm technology were resolved in the project, including a novel UV light based final cleaning technology, new on-line monitoring methods, environment friendly plasma technology to reduce perfluorocarbons in etch process waste, continuous infrared monitoring of organic contamination, and supercritical carbon dioxide cleaning for porous low-k materials. Significant progress was also made in measurement techniques, modelling and understanding of the influence of airborne contamination on the various process steps.

Driving down feature size at a cost

In 2003, the semiconductor industry reached the nano scale by introducing sub-100 nm transistor features. The most advanced microprocessors today are already being produced with 45 nm technologies. Current R&D is now developing the technologies for 32 and 22 nm nodes – and 6 nm critical dimensions have been achieved in laboratories.

However these advances come at a price. The cost of designing new chips is growing at 50% with each new technology generation. This is caused by the increased penetration of software within the chips, the complexity of simulating physical behaviour in complex devices, and the increased number of gates being integrated. The design cost for new chips in 130 nm technology incorporating 9 million gates per chip was €9 million, the cost of a 90 nm chip with 16 million gates was €18 million, and for a 65 nm chip with 30 million gates, the cost is around €46 million.

Similar increases affect the cost of process development as the complexity of the manufacturing process inevitably augments as feature sizes reduce. This is due to the appearance of new materials, assemblies and physical effects that require additional R&D before mass manufacture is possible.

The cost of developing the 90 nm process is put at around €400 million, while the 45 nm process is estimated to cost €600 million – and the 32 nm process may well cost upwards of €800 million.

Enabling industrialisation

From the beginning of MEDEA+, an important strand of the research programme has been in developing the enabling technologies for ever smaller devices ahead of market needs. This was essential to retain and build European competitiveness not only in the different types of components to be fabricated – analogue and digital, logic and memory, and both low and high power – but also in supply of equipment, materials and test systems for global microelectronics manufacture.

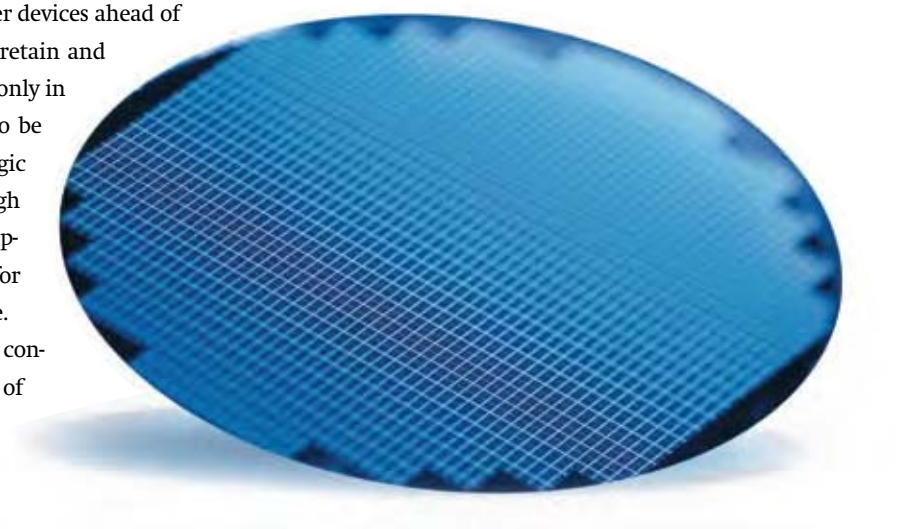
MEDEA+ projects have made major contributions to the industrialisation of submicron CMOS chips. As a result, 90 nm node technology is already in widespread use. The 65 nm node is reaching the product prototyping stage and first choices for a 45 nm technology are available with work continuing towards full process integration well in line with the International Technology Roadmap for Semiconductors (ITRS).

Work on submicron chips started with the MEDEA+ T201 CMOS logic 0.1 μm project that developed the process rules for industrial exploitation of 90 nm CMOS industrial technology. The project covered lithography, improved substrate materials and metallisation, as well as device architecture optimisation.

In the year after the project, some 25 submicron chips were processed successfully, demonstrating design efficiency and optimum use of technology and manufacturing capabilities. Products included digital, analogue, radio-frequency (RF) and embedded memory devices for diverse applications, such as wireless handsets, TV set-top boxes and networking components.

Achievements of the CMOS logic 0.1 μm project set the stage for the successful development of 65 nm processes through the MEDEA+ T207 65 nm CMOS300 project, which involved new substrate materials as well as multilevel interconnect metallisation for 65 nm circuit nodes. The 65 nm process was established with significant yield improvements and reliability meeting specifications, and was ready for the manufacture of prototype customer chips at the end of 2005.

The chipmaking partners involved in the project were able to share their 65 nm cell libraries and IP blocks and were confident about the success of the process for full production from 2008.



Speeding up 45 nm production

Full CMOS integration at the 45 nm feature level was the subject of the MEDEA+ 2T103 FOREMOST project that set out to develop the necessary abilities in Europe ahead of the ITRS, which called for 45 nm node product shipments by 2010.

FOREMOST built on the outcome of the EU Framework Programme NANOCMOS project, which achieved a first demonstration of feasibility of a suitable logic process in 2005. This was based on a selection of the most appropriate technology among the several options studied.

The main objective of FOREMOST is to demonstrate a full CMOS 45 nm process technology in European 300-mm wafer manufacturing facilities. The proposal targeted both CMOS logic and DRAM/flash memory process technologies, and promoted synergy between the competences of the then Crolles 2 Alliance in Grenoble and Qimonda in Dresden, Germany. It should demonstrate the feasibility of a complex test vehicle representative of 45 nm design rules that are three times more complex than the most complex current 90 nm design.

And MEDEA+ projects were planned to exploit further the results of the EU Framework Programme NANOCMOS and PULLNANO projects that are both looking further ahead at the needs for 32/22 nm scale circuitry.

Boost to substrate engineering

In parallel with developing new processing steps, MEDEA+ also investigated new substrate materials as the limits of bulk silicon were being reached.

The MEDEA+ 2T101 SilOnIS project intended to develop large diameter strained silicon-on-insulator (SOI) substrates and speed their introduction in full scale production for below 65 nm half pitch CMOS devices. Strained silicon offers higher speeds and lower consumption than bulk silicon, while SOI fabrication improves performance further. The project built on the strengths of the main European players in substrates, chipmaking and metrology to combine high mobility wafer-level strained silicon and SOI in a single technology platform for high performance chips.

As a result of SilOnIS, industry-standard 300-mm diameter wafers of thin and thick strained SOI prototype substrates were delivered to the chipmaking partners for device development. These wafers could be used in existing processing equipment. A particular advantage is that the MEDEA+ project addressed more than one ITRS node with multiple reuse of results possible as dimensions continue to reduce.

And suitable wafers have been demonstrated targeting device fabrication at the 45 nm half-pitch node and below, in line with global industry needs. Suitable wafers are already being made available commercially for 45 nm technology fabrication.

While SilOnIS was device led, it required innovations at both material and substrate levels. It also marked a first step in the engineering of advanced substrates for integrated circuit production. By supporting work in this area, SilOnIS participated in the recognition of a field of activity that can become another future European strength. The results has not only boosted the companies involved directly but also the ecosystems with which they are involved, benefiting employment and spreading knowhow in this important field.

The work was taken further in the MEDEA+ 2T104 DECISIF project that set out to integrate performance boosters in fully and partially depleted SOI technologies for low power and high performance, to validate their impact by fabricating complex 45 nm node demonstrators directly comparable with bulk silicon and to develop design kits and SOI-adapted circuit design for the evaluation by application designers.

Improving device yields

The MEDEA+ 2T102 HYMNE project set out to develop methods, software and hardware that enable European chipmakers to shorten production cycle times and improve device yields, through increased automation and use of new materials. Project work has been split into three parts:

1. Factory management and automation implementing advanced techniques to improve yield and cycle time by building a coherent framework to streamline volume production management, reduce time to volume and optimise introduction of new products and technologies to reduce time to market;
2. Supply of new materials and contamination-free wafer handling to cut the time for integration of new process modules, materials and chemistry for sub-65 nm CMOS high volume production. This includes developing facilities and tool-cleaning procedures to reduce wafer contamination as well as new material precursors and slurries for chemical mechanical polishing for 65 and 45 nm technologies; and
3. Zero-defect and advanced yield learning involving examination and elimination of systematic and random defects from new materials, processing tools and processing methods for sub-65 nm technologies that affect yields.

Looking ahead

Mastering process technology is a prerequisite to ensure chip are designed quickly and are right first time. The CATRENE nanoelectronics Cluster – the successor to MEDEA+ – will continue the goal of obtaining full mastery of the processes involved. Future work will include determining the process innovations and new materials needed to meet new challenges in device and process integration.

MEDEA+ Office
140bis, Rue de Rennes – F-75006 Paris – France
Tel.: +33 1 40 64 45 60 – Fax: +33 1 40 64 45 89
Email: medeaplus@medeaplus.org
http://www.medeaplus.org

MEDEA+ ∑!2365 (2001 to 2008) was the industry-driven pan-European programme for advanced co-operative R&D in microelectronics. Its aim was to make Europe the global leader in systems innovation on silicon. Some 90 projects were labelled, covering challenges in microelectronics applications and enabling technologies, and involving 2500 scientists and engineers annually from 23 European countries. The more than 600 partners included major microelectronics manufacturers, systems houses, SMEs, universities and institutes.